

REMARKS

Applicant hereby traverses the outstanding rejections and request reconsideration and withdrawal in view of the remarks contained herein. Claims 1-10 have been previously canceled. Claims 11-17 have been withdrawn from consideration. Claims 18-29 are pending in this application.

Notice to Correct

In response to the Notice to Correct, Applicant has included a listing of the withdrawn claims omitted from the original response.

Interview Summary

Applicant participated in a telephonic interview with Examiner Torres on Monday December 12, 2005. Applicant discussed the pending action and restriction requirement with the Examiner. In view of the interview and the Petition of Restriction Requirement dated August 3, 2005, the Examiner agreed to remove the restriction requirement and issue a non-final office action examining claims 18-29. Applicant reserves the right to petition to reinstate the appeal if, under some circumstance, the Examiner does not issue a non-final office action on claims 18-29.

Applicant thanks Examiner Torres for his time and consideration in this matter.

Restriction Requirement

Applicant respectfully asserts, that in view of the interview of December 12, 2005, the restriction requirement in the present office action is moot. If the Examiner maintains the restriction requirement, Applicant reserves the right to reinstate the Petition of Restriction Requirement filed August 3, 2005.

Rejection under 35 U.S.C. § 103

Applicant believes that a response to the present office action on the merits is not required in view of the interview with the Examiner on December 12, 2005, however, in order to insure that Applicant responds fully to all outstanding issues, Applicant is repeating the arguments made with respect to claims 18-20 in the Appeal Brief filed August 3, 2005.

Claims 18-20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over United States Patent Number 4,939,694 to Eaton et al. (hereinafter "Eaton) in view of United States Patent Number 4,460,997 to Harns (hereinafter "Harns").

To establish a *prima facie* case of obviousness, three basic criteria must be met, see M.P.E.P. § 2143. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Without conceding the first or second criteria, Applicant respectfully asserts that the combination does not teach all of the claim limitations of claims 18 and 19.

Claim 18 defines a method that includes determining a number of said identified faulty ones of said evaluated elements in each plurality of subsets of said memory segments and physically re-mapping said memory segment in response to said declared failure condition. The Examiner does not dispute that Eaton discloses a memory system that is operable to logically remap defective memory locations to replacement memory locations using substitute memory table 3-11. (column 5, lines 16-19) The substitute memory table of Eaton can either be a look-up table for all memory locations, or a content addressable memory to look up only replaced memory locations. (column 5, lines 20-40 and column 7, lines 21-28) In either case, Eaton's only disclosed means of replacing defective memory locations requires a mapping function in some type of memory, meaning that Eaton logically remaps defective memory cells, in contrast to the physical re-mapping of claim 18. Harns is not relied upon as teaching the remapping of defective memory locations.

In the Advisory Action dated January 3, 2005, the Examiner states:

Any time a logical memory location is remapped so is the physical memory location corresponding to the logical and physical memory locations. The Examiner asserts that if a logical memory location is found faulty, then the physical memory location corresponding to the logical memory location is faulty; hence remapping of the logical memory location corresponding to the physical memory location allows the logical memory location corresponding to the physical memory location to be remapped to a replacement logical

memory location corresponding to the replacement physical memory location. What good would it do to remap the logical memory location and not the physical memory location corresponding to the logical memory location since it is the physical memory location that is faulty? A one to one mapping between physical location and logical location ensures that the logical locations are substantially the physical locations as well.

Most importantly, the Examiner concludes: "Hence Eaton teaches remapping defective physical memory locations."

The present invention includes "physically re-mapping", which has very different implications than the Examiner's mischaracterization of "remapping defective physical memory locations." When a defective memory location is logically remapped the defective physical memory location still has the same physical address lines which can still be used to physically address the defective memory location. The same cannot be said for the "physical re-mapping" of the present invention.

The combination of Eaton and Harns does not teach or suggest each and every feature of claim 18 and claim 19 through its dependency from claim 18. Therefore, claim 18 is patentable over the rejection of record.

Claim 20, through its dependency on claim 18, defines a method that includes determining a number of said identified faulty ones of said evaluated elements in each plurality of subsets of said memory segments and physically re-mapping said memory segment in response to said declared failure condition. Claim 20 further requires incrementing a failure counter upon detection of a faulty memory element in the step of identifying. Again, the Examiner does not dispute that Eaton discloses a memory system that is operable to logically remap defective memory locations to replacement memory locations using substitute memory table 3-11. (column 5, lines 16-19) Eaton logically remaps defective memory cells, in contrast to the physical re-mapping of claim 20, and Harns is not relied upon as showing the limitation.

Further, the Examiner admits that "Eaton and Harns do not explicitly teach the specific use of a failure counter." While Eaton maintains the number of defective symbols in

each record as cited by the Examiner at column 7, lines 14-17, Eaton does not disclose incrementing a failure counter upon detection of a faulty element as set forth in claim 20.

For the reasons set forth above, the combination of Eaton and Harns does not teach every element of claim 20, therefore claim 20 is patentable over the rejection of record.

Conclusion

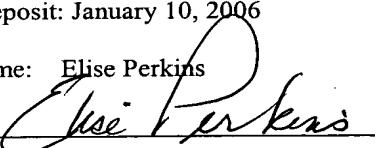
In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

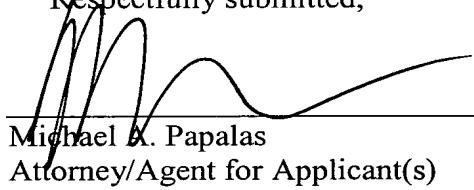
Applicant believes no fee is due with this response. However, if a fee is due, please charge Deposit Account No. 08-2025, under Order No. 10004546-1 from which the undersigned is authorized to draw.

I hereby certify that this correspondence is being deposited with the United States Postal Service as Express Mail, Label No. EV482726331US in an envelope addressed to: MS Amendment, Commissioner for Patents, Alexandria, VA 22313.

Date of Deposit: January 10, 2006

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